Comprehensive Analog Layout Constraint Verification for Matching Devices

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Motivation

In most analog designs, including analog IPs, analog and analog-mixed-signal ICs, designers must take into account each device's relative accuracy to reduce the variability of functions and characteristics. Layout designers must also consider the size and placement of those devices that require matching dependencies on the layout.

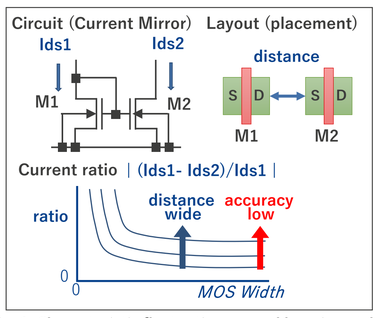


Fig. 1. Characteristic fluctuation caused by mismatch.

- **The importance of guaranteeing relative accuracy**
  - Fig. 1 shows a current mirror circuit commonly used in analog design. Current ratio of these two transistors must be matched for expected operation.
  - Because the current ratio is varied by the distance between devices, the layout designer must place devices in compliance with spacing and the other geometrical rules so the layout can meet the required current ratio accuracy.

- **Requires many device matching constraints to ensure relative accuracy**
  - Fig. 2 shows that there are many layout constraints that matched devices should comply with.
  - Device matching constraints apply to MOS transistors, bipolar transistors, resistors and capacitors.
  - The total number of constraint verifications is *over a thousand*.

#	Constraint Types
1	Parameter Matching
2	Diffusion Area Matching
3	LOD Effect Matching
4	Placement Order
5	Placement Direction
6	Placement Adjacent
7	Placement Interval
8	Placement SideDummy
9	OS Effect Matching
13	..*Many constraint types !!*

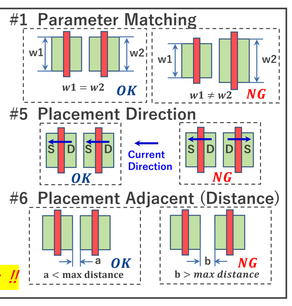


Fig. 2. Example of device matching constraint.

- **Most device matching constraints are manual checks**
  - Currently, these constraints were checked manually, requiring significant time and effort.
  - Its man-hours has *over a month* per product.

- **Requires a new approach of device matching constraint verifications**
  - Fig. 3 shows the constraint verification flow in the current design flow.
  - All verifications of device matching constraint are manual checks that have *high risk of human error* such as verification omission and false check.
  - So layout design may require a major rework by constraint violations.
  - As a new approach, we needed to improve the quality and efficiency of analog designs by automating device matching constraint verifications, which is currently considered difficult.

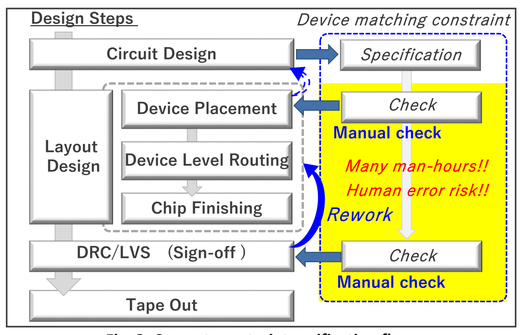


Fig. 3. Current constraint verification flow.

Requirements for Device Matching Verification

- The requirements for automated device matching constraint verification to improve analog design quality and efficiency are ①Comprehensiveness, ②Constraint type coverage, ③Early stage verification, ④Short TAT and ⑤Ease of expansion.
- We compared existing technologies and concluded that no tool or technique satisfies all requirements about device matching constraint verifications (Table I).

TABLE I COMPARISON OF DEVICE MATCHING CONSTRAINT VERIFICATIONS

No.	Requirements		LVS	DRC	Pattern Matching	Manual Check
①	Comprehensiveness	Verify all constraint without exception	✔	✔	✔	-
②	Constraint type coverage	Cover all constraint types of device matching	-	-	-	-
③	Early stage verification	Verify before LVS clean (In-design verification)	-	✔	✔	✔
④	Short TAT	Less than 4h	✔	✔	✔	-
⑤	Ease of expansion	Apply to new process with minimum effort	-	-	✔	✔

- We evaluated Calibre® PERC™ then it satisfies followings required to “Constraint type coverage”.
  (A) Identify which devices should be matched and verified
  (B) Derive device parameters to compare with constraint value
  (C) Derive device geometries to compare with constraint value
- However, Calibre® PERC™ platform alone can not cope with No. ③ and No. ⑤ of requirements.

System Configuration

Fig. 4 shows system configuration of newly developed device matching constraint verification.

- **Comprehensiveness(①) and Constraint type coverage(②)**
  These requirements have realized by developing a Calibre® PERC™ Rule Deck files that covers all necessary constraint types for every device type. And “Matched Device Constraint” data extract devices and matching constraints from constraints (OA) using current systems.

- **Early stage verification (In-design verification)(③)**
  This requirement has realized by developing a generation tool of “Matched Device Location” data. “Matched Device Location” data use the current system to extract correspondences between schematic instances and layout devices from Schematic (OA), Layout(OA) and Constraint(OA).

- **Short TAT(④)**
  This requirements have realized by developing a Calibre® PERC™ Rule Deck files that generated a subset DB from layout DB.

- **Ease of expansion(⑤)**
  This requirements have realized by developing a Calibre® PERC™ Rule Deck files that can control with process setup file.

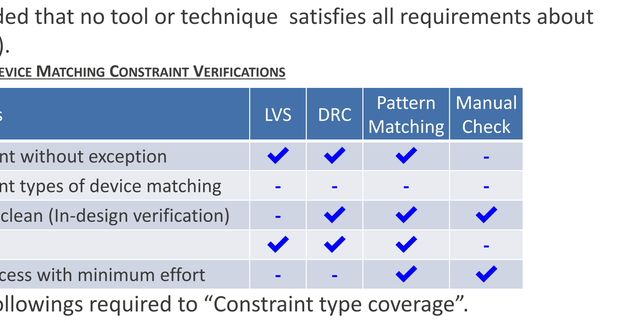


Fig. 4. System Configuration.

Early Stage Verification and Ease of Expansion

In the verification flow of device matching constraint, the flow checks whether parameters and geometries of the matched devices have satisfied the constraint or not. (Fig. 5)

- **Early stage verification (In-design verification) (③)**
  Layout devices cannot be associated with schematic instances on Calibre PERC® platform in in- design phase. Usually, LVS is utilized for identifying devices in sign-off phase. We resolved this issue by introducing “Matched Device Location” which has device locations of schematic instances.

- **Ease of expansion (⑤)**
  Usually, Calibre PERC® Rule Deck should be developed for each processes.
  In order to support various processes easily, we divided the deck into procedure part and process dependent part. The process dependent constraint rule should be defined in “Process Setup file”.

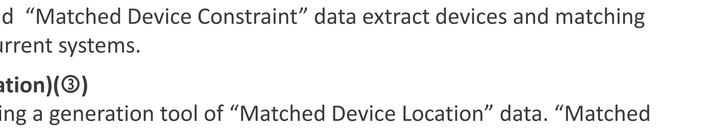


Fig. 5. Device Recognition in the Verification Flow.

Short TAT

- Using the advanced geometry analysis capabilities of the Calibre® PERC™ tool, we successfully recognized which data is required by any of the matching constraints through sequential data filtering, and created a subset DB.
- The verification time is shorter, since we no longer need to repeat data extraction and the system accesses the subset DB during the verification (Fig. 6).

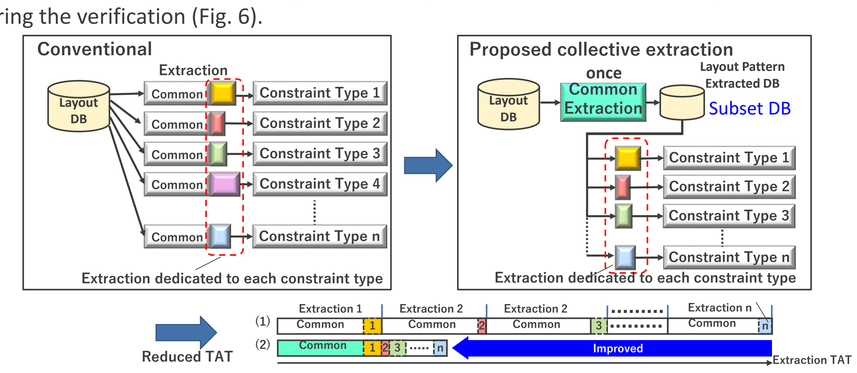
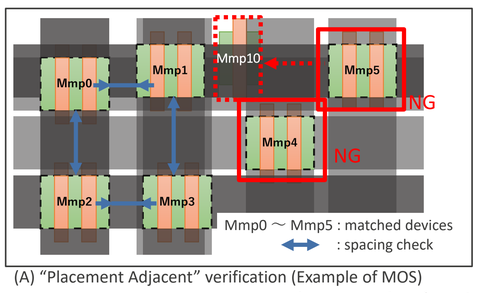


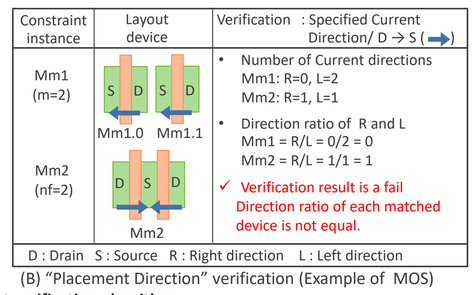
Fig. 6. Device information extraction.

Constraint Verification Algorithm

- The verification algorithm of “Placement Adjacent” and “Placement Direction” constraints which are frequently specified in actual design are shown below (Fig. 7).
  (A) “Placement Adjacent” verification is judged the horizontal and vertical projection overlap amount and distance for the recognition pattern of each matched device.
  (B) “Placement Direction” verification recognizes first the number of directions in the same and the opposite to the specified current direction for each matched device, and judges the ratio of the number of the same direction and the opposite direction.



(A) “Placement Adjacent” verification (Example of MOS)



(B) “Placement Direction” verification (Example of MOS)

Fig. 7. Examples of constraint verification algorithm.

Example of Verification

- Fig. 8 shows the example of the verification results of actual design. “Diffusion Area Matching”, “LOD Effect Matching” and “Placement Direction” constraints are FAIL for the constraint members No.3.

No	Constraint Members	Result	Parameter	DiffArea	LODEffect	Order	Direction	Adjacent	Interval	SideDummy	OSEffect
1	MMP49 MMP51 MMP53 MMP55 MMP58 MMP60	pass	pass	pass	pass	-	pass	pass	pass	pass	pass
2	MMP11 MMP14 MMP17 MMP19 MMP29 MMP65 MMP8	FAIL	pass	FAIL	FAIL	-	FAIL	pass	pass	pass	pass
3	MMN11 MMN16 MMN26 MMN8 MN9	FAIL	pass	FAIL	FAIL	-	FAIL	pass	pass	pass	pass
4	MMN28 MMN40	FAIL	pass	pass	pass	-	FAIL	pass	pass	pass	pass
5	MMP32 MMP42	pass	pass	pass	pass	-	pass	pass	pass	pass	pass
6	MMP0 MMP1 MMP2 MMP3	pass	pass	pass	pass	-	pass	pass	pass	pass	pass
7	MMN0 MMN1 MMN2 MMN3	pass	pass	pass	pass	-	pass	pass	pass	pass	pass

Fig. 8. Examples of constraint verification result.

- “Diffusion Area Matching” checks matching of the ratio of source diffusion area to drain diffusion area.
- “LOD Effect Matching” checks matching of the average of SA and SB of each devices.
- “Placement Direction” checks matching of the ratio of the current direction from drain to source.
- The evaluated numbers of each constraint are shown in Table II. The numbers of each constraints are mismatched.
- Then, these three constraints become FAIL.

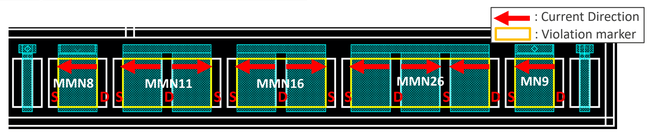


Fig. 9. Layout violated constraints.

TABLE II THE EVALUATED NUMBERS OF EACH CONSTRAINT

	MMN8	MMN11	MMN16	MMN26	MN9
Diffusion area ratio (Drain/Source)	1	0.5	0.5	1	1
SA and SB	1	3.5	3.5	6	1
Current direction	L:1, R:0	L:1, R:1	L:1, R:1	L:2, R:1	L:1, R:1

Evidence

- All types of matching constraints checking functions have been successfully implemented (9 generic and 4 Renesas-specific).
- We ran chip-level verification on 90nm design and checked 2,208 (Table III, Table IV, Fig. 11). It took only 1 hour, faster than our target TAT (4 hours).
- The verification man-hour was reduced by 80% compared with manual verification in 180nm mixed-signal block designs (Fig. 10). It detected many current direction violations that cannot be detected by a manual solution.
- This system was released internally and being applied to production designs.

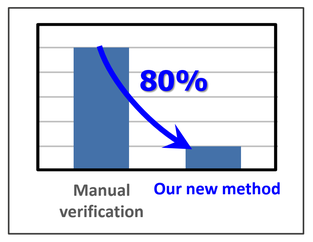


Fig. 10. Verification man-hour reduction.

TABLE III VERIFICATION TAT

Summary	
Process	90nm
Product category	Motor Driver
Number of Elements	36K
Number of Specified Device Matching Constraint	254(group)
Number of Specified Verifications	2,208
Run time of Verifications	1 hour

TABLE IV THE NUMBER OF VERIFICATION ITEMS

#	Constraint Type	Verifications
1	Parameter Matching	228
2	Diffusion Area Matching	204
3	LOD Effect Matching	204
4	Placement Order	28
5	Placement Direction	176
6	Placement Adjacent	228
7	Placement Interval	0*
8	Placement SideDummy	228
9	OS Effect Matching	228
10-13	Renesas-specific	684

*This constraint type is supported in the latest version

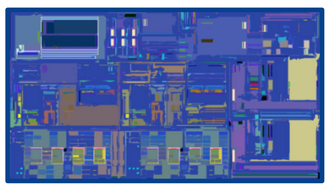


Fig. 11. Chip layout of 90nm design.

Summary

Conclusion

- Fully automated analog layout verification system for matched devices was successfully developed with Calibre® PERC™. (Table V)
- Already applied to 3 analog-mixed-signal IC production designs in automotive and other markets and detected constraint violations as expected.
- Proved that this system significantly reduces human error risks and verification man-hour by 80%.

TABLE V RESULT OF DEVELOPMENT

Requirements	This work with Calibre® PERC™	
Comprehensiveness	Automatic Verification of Matching Constraint	OK
Constraint type coverage	Covered all of 13 constraint types	OK
Early stage Verification	In-Design Verification was supported	OK
Short TAT	Achieved target by collective extraction	OK
Ease of expansion	Separated process set up file	OK

Future work

- Add wiring matched constraint verifications.
- More shorten the verification TAT.